REMARKS

Claims 43-66, 98-103, 106 and 107 are pending in this application.

Claims 45, 60-66 and 99-102 are rejected under 35 U.S.C. 112.

Claims 50, 98 and 101 are objected to because of informalities.

Claims 43, 47, 48, 50, 51, 53, 57 and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto.

Claims 44, 46, 55, 56, 98, 106 and 107 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined device of Sakamoto in view of Bulucea et al.

Claims 49 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Davies.

Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Blanchard.

Reconsideration is requested. Claims 43, 50, 52, 65, 66, 98, 99, 100, 101 and 103 are amended. Claims 44-46, 67-97, 102 and 104-107 are canceled.

Objections to the Drawings

FIGS. 6B and 6C are objected to. FIG. 6B is objected to as it does not match FIG. 19 of U.S. Pat. No. 4,895,810. FIG. 6C is objected to as it does not match FIG. 16B of U.S. Pat. No. 5,262,336. The drawings of Figs. 6B and 6C are corrected and a new drawing is submitted herewith.

Rejections Under 35 U.S.C. § 112

Claims 45, 60-66 and 99-102 are rejected under 35 U.S.C. 112, para 1. This rejection is traversed.

As to claim 45, the Examiner asserts that the specification never disclosed a portion of the upper metal as claimed in claim 44 also contacts the source conductor as claimed in claim 45 and states that such structure would create a short circuit between the source electrode and gate electrode.

Claims 44 and 45 are canceled and limitations thereof are added to claim 43, with amendments to overcome this rejection. Specifically, the language from claim 45 is amended

to specify that a second portion of the upper metal layer is coupled to the source region in electrical isolation from the gate conductor; i.e., no short circuit exists between the source and gate electrodes. Support for the claimed subject matter is found in the specification at page 14, lines 19-28 and page 16, lines 1-4, and in Figs. 12 and 13 cited therein. Further support is found in incorporated-by-reference U.S. Pat. No. 5,262,336 at col. 15, lines 8-14 and 51-54, and Fig. 18.

Accordingly, claim 43—now incorporating claim 44 and 45 amended as discussed above, is allowable under 35 U.S.C. §112 para. 1.

As for claims 60-66 and 99-102, the Examiner asserts that the specification never discloses the gate electrode of Fig. 6B can also be applied to the gate electrode of a trench-type gate MOSFET. It is correct that the specification explicitly mentions refractory metal deposition at page 11, line 27 to page 12, line 1. However, this text also specifically identifies the purpose of doing so---to further reduce gate resistance--and the preceding text (page 11, line 3) references applicant's prior U.S. Pat. No. 4,895,810 (incorporated by reference at page 14, lines 13-14). The '810 patent, at col. 12, lines 25-34, describes applying a metal layer of substantial conductivity, such as tungsten on the polysilicon layer. Silicide formulation is described as an alterative. The '810 patent then describes (at col. 12, lines 47-56) applying added metal by "many methods including plating, evaporation and sputtering." Use of aluminum is mentioned at line 54, and described in detail at col. 10, lines 22-31. Col. 13, lines 9-12, make clear that metallization over the polysilicon is preferred for high speed devices.

Applicant's U.S. Pat. No. 5,262,336 is also incorporated by reference at page 9, lines 15-17. At col. 26, lines 64-65, it recites "a deposition temperature of 430°C" for the passivation layer, supporting claim 101.

It should also be noted that--although the Examiner refers to Fig. 6B as showing a planar gate type MOSFET--Fig. 19 of the '810 patent in fact shows a shallow trench (see Examiner's objection to Fig. 6B, and new Fig. 6B corrected to match '810 Fig. 19). Moreover, this application specifically states, at page 20, lines 3-8, that both types of device can be formed on the same die in the manner described in the commonly-assigned patents ('810 and '336).

In view of these facts, as well as applicant's express incorporation by reference of the commonly-owned '810 patent and '336 patent, also showing aluminum on gate polysilicon in

a trenched MOSFET structure, a person skilled in the art would readily understand and be able to apply the teachings supporting claims 60-66 and 99-102. Accordingly, these claims are allowable under 35 U.S.C. § 112, para 1.

Objected To Informalities

Claims 50, 98 and 101 are objected to because of informalities. Claims 50 and 98 and 101 are amended to correct the indicated informalities.

Rejections Under 35 U.S.C. § 103(a)

Claims 43, 47, 48, 50, 51, 53, 57 and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto and claims 44, 46, 52, 55 and 56, 98, 103, 106 and 107 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined device of Sakamoto in view of Bulucea et al.

Claim 43 is amended to include selected limitations from claims 44 and 45, as mentioned above. Claims 44-46 are canceled.

Sakamoto does not disclose or suggest the combination of a metallized gate polysilicon, an insulating layer over the gate conductor, and an upper metal layer over the insulating layer and having a first portion contacting the gate conductor through a via and a second portion contacting the source region in electrical isolation from the gate conductor. The Examiner acknowledges as much in the Action at page 6, lines 4-6.

Bulucea does not disclose a metallized gate polysilicon layer as claimed. The Examiner cites Bulucea as showing an insulating layer over the gate conductor [36a, 36b] and an upper metal layer [43a] contacting the gate conductor through a via in the insulating layer. However, closer examination of Bulucea Figs. 21-31B shows that the metal layer 43a only contacts the doped polysilicon layer [36b] through a via in the insulator in the Termination Region; no contact is made to doped polysilicon layer [36a] in the Active Region. See Bulucea Fig. 31A. Bulucea, therefore, does not disclose a gate conductor comprising a metal layer overlying the doped polysilicon layer of the gate conductor. Accordingly, independent claim 43 should be allowable over Sakamoto and Bulucea.

The remaining claims depending from claim 43 should likewise be allowable. It is noted that claims 60-66 are not rejected under Sections 102 or 103; only under Section

112(1), which rejection is answered fully above. In particular, claims 60, 64 and 65 specify gate metal overlying the doped polysilicon as comprising aluminum, which is taught in neither Sakamoto nor Bulucea. Claim 64 further specifies the upper metal layer as aluminum, likewise not taught in either Sakamoto or Bulucea. Accordingly, these claims should be allowable in their own right.

Claims 49 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Davies, and claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Blanchard. However, none of Sakamoto, Davies or Blanchard disclose or suggest the subject matter of amended claim 43. Accordingly, dependent claims 49, 54 and 59 are allowable with claim 43.

Claims 98, 103, 106 and 107 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined device of Sakamoto in view of Bulucea et al.

Claim 98 is amended similarly to recite an insulated gate power MOSFET device in which the conductive gate structure includes a first portion of a first metal layer over the doped gate polysilicon, a second portion of the first metal layer over the source semiconductor material, an insulating layer over the gate structure and between the first and second portions of the first metal layer, and a second metallization over the insulating layer, having a first portion contacting the first portion of the first metal layer through the insulating layer and a second portion contacting the second portion of the first metal layer.

As noted above, the Examiner acknowledges that Sakamoto does not show an insulating layer over the gate conductor and an upper metal layer over the insulator contacting the gate conductor through a via in the insulator. The Examiner cites Bulucea as showing an insulator layer over the gate conductor and an upper metal layer over the insulating layer and contacting the gate conductor through a via. As explained above, Bulucea does not disclose a metal layer (aluminum) having a portion extending over the doped polysilicon overlying the gate oxide layer in the Active Region.

Accordingly, claim 98 is allowable over Sakamoto and Bulucea, along with its dependent claims 99-101 and 103.

In view of the foregoing amendments and remarks, the application should now be allowable. If there are any questions, the Examiner is requested to call the undersigned.

Respectfully submitted,

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In the drawings:

Please replace Fig. 6B and Fig. 6C in the application with the enclosed replacement sheet containing revised Fig. 6B and 6C.

Revised Fig. 6B is a copy of Fig. 19 of U.S. Pat. No. 4,895,810, with reference numerals changed to match those of prior Fig. 6B.

Revised Fig. 6C is a copy of Fig. 16B of U.S. Pat. No. 5,262,336, with reference numerals changed to match those of prior Fig. 6C.